**文件源：PHY Interface For the PCI Express, SATA, and USB 3.1 Architectures，Version 4.4**

**8.3 Power Management – PCI Express Mode**

**8.3 电源管理——PCI Express 模式**

The power management signals allow the PHY to minimize power consumption. The PHY must meet all timing constraints provided in the PCI Express Base Specification regarding clock recovery and link training for the various power states. The PHY must also meet all terminations requirements for transmitters and receivers.

电源管理信号允许 PHY 最大限度地降低功耗。 PHY 必须满足 PCI Express 基本规范中提供的有关时钟恢复和各种电源状态链路训练的所有时序约束。 PHY 还必须满足发射器和接收器的所有端接要求。

Four standard power states are defined, P0, P0s, P1, and P2. P0 state is the normal operational state for the PHY. When directed from P0 to a lower power state, the PHY can immediately take whatever power saving measures are appropriate. A PHY is allowed to implement up to 4 additional PHY specific power states. A MAC may use any of the PHY specific states as long as the PCI Express base specification requirements are still met

定义了四种标准电源状态：P0、P0s、P1 和 P2。 P0 状态是 PHY 的正常操作状态。当从 P0 引导至较低功耗状态时，PHY 可以立即采取任何适当的省电措施。 PHY 最多可以实现 4 个附加 PHY 特定电源状态。只要仍满足 PCI Express 基本规范要求，MAC 就可以使用任何 PHY 特定状态

In states P0, P0s and P1, PCLK is required to be kept operational. For all state transitions between these three states and any PHY specific states where PCLK is operational, the PHY indicates successful transition into the designated power state by a single cycle assertion of PhyStatus. Transitions into and out of P2 or a PHY specific state where PCLK is not operational are described below. For all power state transitions, the MAC must not begin any operational sequences or further power state transitions until the PHY has indicated that the initial state transition is completed

在 P0、P0s 和 P1 状态下，PCLK 需要保持运行。对于这三种状态之间的所有状态转换以及 PCLK 运行的任何 PHY 特定状态之间的所有状态转换，PHY 通过 PhyStatus 的单周期断言指示成功转换到指定电源状态。下面描述了 PCLK 不工作时进出 P2 或 PHY 特定状态的转换。对于所有电源状态转换，在 PHY 指示初始状态转换完成之前，MAC 不得开始任何操作序列或进一步的电源状态转换。

Mapping of PHY power states to states in the Link Training and Status State Machine (LTSSM) found in the base specification are included below. A MAC may alternately use PHY specific states as long as the base specification requirements are still met.

下面包括 PHY 电源状态到基本规范中的链路训练和状态状态机 (LTSSM) 中的状态的映射。只要仍然满足基本规范要求，MAC 就可以交替使用 PHY 特定状态。

* P0 state: All internal clocks in the PHY are operational. P0 is the only state where the PHY transmits and receives PCI Express signaling.

P0 is the appropriate PHY power management state for most states in the Link Training and Status State Machine (LTSSM). Exceptions are listed below for each lower power PHY state.

* P0 状态：PHY 中的所有内部时钟均可运行。 P0 是 PHY 发送和接收 PCI Express 信号的唯一状态。

P0 是适用于链路训练和状态状态机 (LTSSM) 中大多数状态的 PHY 电源管理状态。下面列出了每个较低功耗 PHY 状态的例外情况。

* P0s state: PCLK must stay operational. The MAC may move the PHY to this state only when the transmit channel is idle.

P0s state can be used when the transmitter is in state Tx\_L0s.Idle.

While the PHY is in either P0 or P0s power states, if the receiver is detecting an electrical idle, the receiver portion of the PHY can take appropriate power saving measures. Note that the PHY must be capable of obtaining bit and symbol lock within the PHY-specified time (N\_FTS with/without common clock) upon resumption of signaling on the receive channel.

This requirement only applies if the receiver had previously been bit and symbol locked while in P0 or P0s states.

* P0s 状态：PCLK 必须保持运行。仅当传输通道空闲时，MAC 才可以将 PHY 移至此状态。

当发送器处于 Tx\_L0s.Idle 状态时，可以使用 P0s 状态。

当 PHY 处于 P0 或 P0s 电源状态时，如果接收器检测到电气空闲，则 PHY 的接收器部分可以采取适当的节能措施。请注意，当接收通道上的信令恢复时，PHY 必须能够在 PHY 指定的时间内（带/不带公共时钟的 N\_FTS）获得比特和符号锁定。

此要求仅适用于接收器之前在 P0 或 P0s 状态下被bit锁定和符号锁定的情况。

* P1 state: Selected internal clocks in the PHY can be turned off. PCLK must stay operational.

The MAC will move the PHY to this state only when both transmit and receive channels are idle. The PHY must not indicate successful entry into P1 (by asserting PhyStatus) until PCLK is stable and the operating DC common mode voltage is stable and within specification (as per the base spec).

P1 can be used for the Disabled state, all Detect states, and L1.Idle state (only if L1 substates are not supported) of the Link Training and Status State Machine (LTSSM).

* P1 状态：可以关闭 PHY 中选定的内部时钟。 PCLK 必须保持运行。

仅当发送和接收通道都空闲时，MAC 才会将 PHY 移至此状态。在 PCLK 稳定且工作直流共模电压稳定且符合规格（根据基本规格）之前，PHY 不得指示已成功进入 P1（通过置位 PhyStatus）。

P1 可用于LTSSM（链路训练和状态状态机)禁用状态、所有检测状态和 L1.Idle 状态（仅当不支持 L1 子状态时）。

* P2 state: Selected internal clocks in the PHY can be turned off. The parallel interface is in an asynchronous mode and PCLK is turned off. P2 can be used for the L1.Idle, L2.Idle and L2.TransmitWake states of the Link Training and Status State Machine (LTSSM).
* P2 状态：可以关闭 PHY 中选定的内部时钟。并行接口处于异步模式，PCLK 关闭。 P2 可用于LTSSM(链路训练和状态状态机)的 L1.Idle、L2.Idle 和 L2.TransmitWake 状态。

PCLK as PHY Output: When transitioning into P2, the PHY must assert PhyStatus before PCLK is turned off and then deassert PhyStatus when PCLK is fully off and when the PHY is in the P2 state. When transitioning out of P2, the PHY asserts PhyStatus as soon as possible and leaves it asserted until after PCLK is stable.

PCLK 作为 PHY 输出：转换到 P2 时，PHY 必须在 PCLK 关闭之前断言 PhyStatus，然后在 PCLK 完全关闭且 PHY 处于 P2 状态时取消断言 PhyStatus。当退出 P2 时，PHY 会尽快置位 PhyStatus，并使其保持置位直至 PCLK 稳定后。

PCLK as PHY Input: When transitioning into P2, the PHY must assert PhyStatus for one input PCLK cycle when it is ready for PCLK to be removed. When transitioning out of P2, the PHY must assert PhyStatus for one input PCLK cycle as soon as possible once it has transitioned to P0 and is ready for operation.

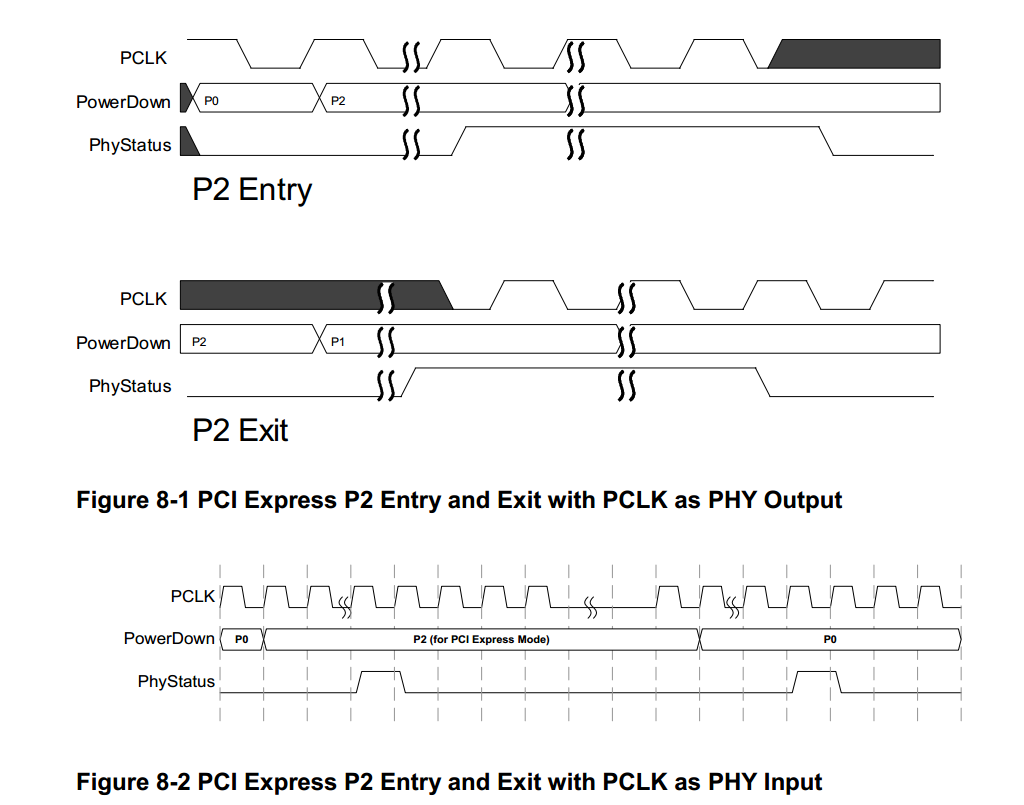
PCLK 作为 PHY 输入：转换到 P2 时，当准备好移除 PCLK 时，PHY 必须在一个输入 PCLK 周期内断言 PhyStatus。当从 P2 转换出来时，一旦转换到 P0 并准备好运行，PHY 必须尽快在一个输入 PCLK 周期内断言 PhyStatus。

When transitioning out of a state that does not provide PCLK to another state that does not provide PCLK, the PHY asserts PhyStatus as soon as the PHY state transition is complete and and leaves it asserted until the MAC asserts AsyncPowerChangeAck. Once the MAC asserts AsyncPowerChangeAck the PHY deasserts PhyStatus.

当从不提供 PCLK 的状态转换到不提供 PCLK 的另一个状态时，一旦 PHY 状态转换完成，PHY 就会断言 PhyStatus，并使其保持断言状态，直到 MAC 断言 AsyncPowerChangeAck。一旦 MAC 置位 AsyncPowerChangeAck，PHY 就会取消置位 PhyStatus。

PHYs should be implemented to minimize power consumption during P2 as this is when the device will have to operate within Vaux power limits (as described in the PCI Express Base Specification)

应实施 PHY 以最大程度地减少 P2 期间的功耗，因为此时设备必须在 Vaux 功率限制内运行（如 PCI Express 基本规范中所述）



There is a limited set of legal power state transitions that a MAC can ask the PHY to make.

Those legal transitions are: P0 to P0s, P0 to P1, P0 to P2, P0s to P0, P1 to P0, and P2 to P0. The base spec also describes what causes those state transitions.

MAC 可以要求 PHY 进行一组有限的合法电源状态转换。

这些合法转换为：P0 到 P0s、P0 到 P1、P0 到 P2、P0s 到 P0、P1 到 P0 以及 P2 到 P0。基本规范还描述了导致这些状态转换的原因。

Transitions to and from any pair of PHY power states including at least one PHY specific power state are also allowed by PIPE (unless otherwise prohibited). However, a MAC must ensure that PCI Express specification timing requirements are met

PIPE(PHY Interface For the PCI Express???) 还允许在任何一对 PHY 电源状态（包括至少一个 PHY 特定电源状态）之间进行转换（除非另有禁止）。然而，MAC 必须确保满足 PCI Express 规范时序要求。

For L1 substate entry, the PHY must support a state where PCLK is disabled, REFCLK can be removed, and RX electrical idle and TX common mode are on; this can be P2 or a P2-like state.

对于 L1 子状态进入，PHY 必须支持 PCLK 禁用、​​REFCLK 可以移除、RX 电气空闲和 TX 共模开启的状态；这可以是 P2 或类似 P2 的状态。

Figure 8-3 illustrates how a transition into and out of an L1 substate could occur. P2 or a P2-like state maps to L1.Idle; and PhyStatus and AsyncPowerChangeAck signals are used as described earlier in this section.

图 8-3 说明了如何发生进入和退出 L1 子状态的转换。 P2或类似P2的状态映射到L1.Idle； PhyStatus 和 AsyncPowerChangeAck 信号的使用如本节前面所述。

